What is claimed is:

1. A semiconductor data processor comprising:

a first memory constituting a cache memory;

a second memory capable of being a cacheable area or a non-cacheable area by the first memory; and

a read buffer capable of carrying out an operation for outputting data corresponding to a read access when the second memory is read accessed as the non-cacheable area.

2. The semiconductor data processor according to claim 1, wherein the read buffer temporarily holds predetermined access data and address when the second memory is accessed as the non-cacheable area.

3. The semiconductor data processor according to claim 2, wherein the read buffer is connected to a first bus at an upstream side of a read request and is connected to a second bus at a downstream side of the read request, and the second bus can transmit data in the number of parallel bits which is equal to or larger than the number of parallel access data bits by the first bus.

4. The semiconductor data processor according to claim 3, wherein the read buffer has a data register for holding read data to be transmitted from the first memory through the second bus, an address register for holding an address of the data, and a control circuit for causing the first bus to output the data of the data register for a read request of an address which

is coincident with the address held in the address register.

5. The semiconductor data processor according to claim 1, wherein the first bus and the second bus are dedicated sequential access buses.

6. The semiconductor data processor according to claim 5, further comprising a third bus capable of connecting the first memory to the second memory in a different path from a path formed by the first and second buses when the second memory is accessed as the cacheable area.

7. The semiconductor data processor according to claim 6, wherein a peripheral bus interface controller is connected to the third bus.

8. The semiconductor data processor according to claim 6, further comprising an internal memory controller connected to the second bus and the third bus and serving to carry out an access interface control for the second memory.

9. The semiconductor data processor according to claim 8, wherein the third bus is provided with a secondary cache memory controller for controlling the second memory as a secondary cache memory for the first memory.

10. The semiconductor data processor according to claim 9, wherein the secondary cache memory controller cache invalidates the second memory in response to a signal indicative of a cache invalidation of the first memory.

11. The semiconductor data processor according to claim

9, further comprising a control register for operably setting the internal memory controller and the secondary cache memory controller exclusively.

12. A semiconductor data processor comprising a first memory constituting a cache memory, a second memory capable of being a secondary cache memory or a memory which is not a cache memory for the first memory, and designating means for selectively designating the second memory to the secondary cache memory or the memory which is not the cache memory.

13. The semiconductor data processor according to claim 12, wherein the second memory has a secondary cache memory controller for carrying out an access interface control as the secondary cache memory of the first memory.

14. The semiconductor data processor according to claim 13, further comprising an internal memory controller for carrying out the access interface control as the memory which is not the cache memory for the second memory.

15. The semiconductor data processor according to claim 14, wherein the designating means is a control register.

16. The semiconductor data processor according to claim 15, wherein the second memory selected to be the memory which is not the cache memory can be a cacheable area or a non-cacheable area by the first memory.

17. The semiconductor data processor according to claim 16, further comprising a read buffer capable of carrying out

an operation for outputting data corresponding to a read access when the second memory is read accessed as the non-cacheable area.

18. The semiconductor data processor according to claim 17, wherein the read buffer newly holds data and an address corresponding to an access if it does not retain data corresponding to the access when the second memory is accessed as the non-cacheable area.

19. The semiconductor data processor according to claim 18, wherein the read buffer is connected to a first bus at an upstream side of a read request and is connected to a second bus having a greater bus width than a width of the first bus at a downstream side of the read request.